

Code No. L0422

R07**Set No.1**

IV B.Tech II Semester Regular Examinations, April, 2011

DIGITAL DESIGN THROUGH VERILOG(Common to Electronics & Communication Engineering, Bio-Medical Engineering and
Electronics & Computer Engineering)**Time: 3 hours****Max.Marks: 80****Answer any FIVE Questions****All Questions carry equal marks**

1. a) Define and explain the following terms pertaining to Verilog HDL.
 - (i) Scalars and Vectors
 - (ii) PLI

[8]
- b) Define and explain the following terms relevant to Verilog HDL language elements.
 - (i) White space characters
 - (ii) Comments
 - (iii) Exercises

[8]
2. a) Describe the following relevant to gate level modeling with necessary syntax and example.
 - (i) Module Structure
 - (ii) Strengths and contention resolution

[8]
- b) Present the gate-level description of a Master-slave Flip-flop circuit with relevant logic diagram and Verilog HDL source code.

[8]
3. a) What are the different kinds of blocks available in Verilog HDL? Explain them with necessary syntax and suitable example.

[8]
- b) Explain the various kinds of Loop statement with necessary syntax and relevant example.

[8]
4. a) Describe the continuous assignment feature of Verilog HDL with suitable example.

[8]
- b) What are the switch level primitives and give their instantiations. Draw the basic switch circuit and its Verilog HDL code.

[8]
5. a) Explain the File-based Tasks and Functions used in Verilog HDL. Briefly discuss them with suitable examples.

[8]
- b) Write notes on modeling a Mealy FSM.

[8]

Code No. L0422**R07****Set No.1**

6. a) What do you mean by State Machine charts? Explain different symbols used in it. How state machine chart differs from a conventional flow chart. [8]
- b) Draw the state diagram and State Machine chart for the synchronous circuit having following description:
- (i) The circuit has control input C, clock and outputs a, b, c.
 - (ii) If C=1, on every positive edge of the clock the output changes in the sequence: 000 → 001 → 011 → 111 → 000 and repeats.
 - (iii) If C=0, the circuit holds in the present state i.e. in the same state. [8]
7. Explain the design flow for FPGAs. By consider suitable example perform the design with the necessary design specifications, logic /state diagram, excitation/state table and relevant Verilog HDL source code. [16]
8. Write a Verilog HDL model that describes the designing of microcontroller CPU with necessary state machine diagram. Test the model using a test bench. [16]

Code No. L0422

R07**Set No.2**

IV B.Tech II Semester Regular Examinations, April, 2011

DIGITAL DESIGN THROUGH VERILOG(Common to Electronics & Communication Engineering, Bio-Medical Engineering and
Electronics & Computer Engineering)**Time: 3 hours****Max.Marks: 80****Answer any FIVE Questions****All Questions carry equal marks**

1. a) Define and explain the following terms relevant to Verilog HDL.
(i) Module (ii) Test bench [8]
b) What first character identifies a system task or a system function? Write a system task to load a 32 by 64 word memory from a data file memA.data. [8]
2. a) Describe the following relevant to gate level modeling with necessary syntax and example.
(i) Gate Delays (ii) Net types [8]
b) Implement the gate-level description of a 9-bit parity generator circuit with relevant logic diagram and Verilog HDL source code. [8]
3. a) What are the primary mechanisms for modeling the behavior of a logic design using Verilog HDL? Explain them with necessary syntax and suitable example. [8]
b) What is the difference between an intra-statement delay and an inter-statement delay? Illustrate with an example. [8]
4. a) Discuss the behavior of the parity encoder circuit using continuous assignment statements. [8]
b) Explain the concept of time delays with switch primitives related to switch level modeling in Verilog HDL. [8]
5. a) Give the list of System Tasks and Functions which are built- in Verilog HDL. Briefly describe them with suitable examples. [10]
b) Write notes on modeling a Moore FSM. [6]

Code No. L0422**R07****Set No.2**

6. a) With an example, explain the concept of alternative realizations for state machine charts using Microprogramming. [8]
- b) Draw the state diagram and state machine chart for a two bit UP/DOWN counter having a control input 'C' in such a way that if $C = 1$ up-counting and $C = 0$ down-counting. The counter should generate an output $Z = 1$ whenever count becomes minimum or maximum. [8]
7. Explain the design flow for Xilinx 3000 series FPGAs. Give the necessary design specifications, logic /state diagram, excitation/state table and relevant Verilog HDL source code. [16]
8. Write a Verilog HDL model that describes the behavior of a simplified 486 bus model with necessary state machine diagram. Test the model using a test bench. [16]

Code No. L0422

R07**Set No.3**

IV B.Tech II Semester Regular Examinations, April, 2011

DIGITAL DESIGN THROUGH VERILOG(Common to Electronics & Communication Engineering, Bio-Medical Engineering and
Electronics & Computer Engineering)**Time: 3 hours****Max. Marks: 80****Answer any FIVE Questions****All Questions carry equal marks**

1. a) What is Verilog HDL? Describe, in brief, the basic modeling styles supported by Verilog HDL. [8]
- b) What are the data types available in Verilog HDL? Discuss them with necessary syntax and an example. [8]
2. a) Describe the following relevant to gate level modeling with necessary syntax and example. [8]
 - (i) Gate delays
 - (ii) Array of Instances
- b) Give a gate-level description of a 2-to-4 decoder circuit with relevant logic diagram and Verilog HDL source code. [8]
3. a) Describe the following relevant to behavioral modeling with necessary syntax and example. [8]
 - (i) Timing controls
 - (ii) Case Statement
- b) Give the behavioral description of a JK Flip-flop circuit using an always statement with necessary logic diagram and Verilog HDL source code. [8]
4. a) Give an example of how turn-off delay is used in a continuous assignment and also present a dataflow model for a 8-bit parameterized magnitude comparator. [8]
- b) Explain about CMOS Switch and Bi-directional Gates related to switch level modeling in Verilog HDL. [8]
5. a) Can a function call a task? Can a task have delays? Illustrate them with suitable examples [8]
- b) Define user-defined primitives with their syntax. Give an example of 4-to-1 multiplexer built using UDPs. [8]

Code No. L0422**R07****Set No.3**

6. a) What is need of state machines? Describe the two basic types of state machines
With proper examples. [8]
b) Discuss about the concepts of ASM charts realization through gates and PLD
devices. [8]
7. Explain the design approach for Altera based complex programmable logic devices.
Give the necessary design specifications, logic /state diagram, excitation/state
table and relevant Verilog HDL source code. [16]
8. Write a Verilog HDL model that describes the interfacing memory to a
microprocessor bus with necessary state machine diagram. Test the model
using a test bench. [16]

UANDISTAR

Code No. L0422

R07**Set No.4**

IV B.Tech II Semester Regular Examinations, April, 2011

DIGITAL DESIGN THROUGH VERILOG(Common to Electronics & Communication Engineering, Bio-Medical Engineering and
Electronics & Computer Engineering)**Time: 3 hours****Max. Marks: 80****Answer any FIVE Questions****All Questions carry equal marks**

1. a) Differentiate the terms 'Simulation' and 'Synthesis' with respect to design considerations. Also give the available Simulation and Synthesis tools. [8]
b) What are the basic logic values available in Verilog HDL? Explain the types of constants in Verilog HDL with necessary syntax and an example. [8]
2. a) What are the built-in primitive gates available in Verilog HDL? Explain how these can be used to describe hardware. [8]
b) Implement the gate-level description of JK flip-flop circuit with relevant logic diagram and Verilog HDL source code. [8]
3. a) Discuss the following related to behavioral modeling with necessary syntax and an example. [8]
(i) Block Statement (ii) Loop Statement
b) What is the difference between a sequential block and a parallel block? Explain using an example. Can a sequential block appear within a parallel block? [8]
4. a) Write a dataflow model for the parity generator circuit. Use only two assignment statements. Specify rise and fall delays as well. [8]
b) Explain the concept of Strength Contention with Trireg Nets related to switch level modeling in Verilog HDL. [8]
5. a) Give the list of standard compiler directives used in Verilog HDL and describe them with an examples. [8]
b) What is meant by Sequential UDP? Explain the various types of sequential UDP with suitable examples. [8]

Code No. L0422**R07****Set No.4**

6. a) Explain the concept of state machine chart realization through MUX and PLD devices. [8]
- b) Draw an ASM chart to describe a state machine that detects a sequence of three logic 1s occurring at the input and that asserts a logic 1 at the output during the last state of the sequence. Write a two-process Verilog HDL description of the state machine. [8]
7. Explain the design flow for Altera based FLEX 10K CPLDs. By considering an example, perform the design with the necessary design specifications, logic /state diagram, excitation/state table and relevant Verilog HDL source code. [16]
8. Write a Verilog HDL model that describes the behavior of UART with necessary state machine diagram. Test the model using a test bench. [16]